

## SHIKSHA CLASSES

	Science X <sup>th</sup> - CBSE	(	<b>Question</b> 12. Electr	Marks : 30 Time : 1 Hour.	
			SECTIO	N (A)	( Each - 1 Marl
Q.1 :	When a current I flows through a resistance R for time 't' the electrical energy spent is give				
	a) IRt	b) I <sup>2</sup> R	t o	c) $IR^2t$	d) I <sup>2</sup> R/t
			OR		$\overline{}$
	If the current flo	wing through	n a fixed resisto	or is halved, the l	neat produced in it will become :
	a) One-fourth	b) On	e-half	c) Double	(d) Four times
Q.2	A wire of resistance $R_1$ , is cut into five equal pieces. These five pieces of wire are then connected in parallel. If the resultant resistance of this combination be $R_2$ , then the ratio $R_1/R_2$ is:				
	a) 1/25	b) 1/5	i d	c) 5	d) 25
			OR	$\mathbf{Q}'$	
				ratio 1:2. If the	ey are joined in series. the energ
	consumed in the $2$			a) 4.1	J) 1.1
	a) 2:1	b) 1:2		c) 4:1	d) 1:1
					eled Assertion (A) and other
				wer to these q	uestions from the codes (a),
	(b), (c) and (d) as	given below		_	
	(b), (c) and (d) as a) Both A and I	<b>given below</b> R are true and	d R is correct e	explanation of th	ne assertion.
	(b), (c) and (d) as a) Both A and I	<b>given below</b> R are true and R are true but	d R is correct e	explanation of th	
	<ul> <li>(b), (c) and (d) as</li> <li>a) Both A and I</li> <li>b) Both A and I</li> </ul>	<b>given below</b> R are true and R are true but R is false.	d R is correct e	explanation of th	ne assertion.
	<ul> <li>(b), (c) and (d) as a</li> <li>a) Both A and I</li> <li>b) Both A and I</li> <li>c) A is true but</li> <li>d) A is false but</li> </ul>	<b>given below</b> R are true and R are true but R is false. t R is true.	d R is correct e t R is not the c	explanation of th orrect explanato	ne assertion. Sin of the assertion.
	<ul> <li>(b), (c) and (d) as a Both A and I</li> <li>b) Both A and I</li> <li>c) A is true but</li> <li>d) A is false but</li> <li>: Assertion (A) : series.</li> </ul>	given below R are true and R are true but R is false. t R is true. The current	d R is correct of t R is not the c t flowing thro	explanation of th orrect explanato ugh each resisto	ne assertion. bin of the assertion. or is the same when connected i
	<ul> <li>(b), (c) and (d) as a Both A and I b) Both A and I c) A is true but d) A is false but</li> <li>Assertion (A) : series.</li> <li>Reason (R) : T parallel.</li> </ul>	given below R are true and R are true but R is false. t R is true. The current he voltage d	d R is correct of t R is not the c t flowing thro rop across ea	explanation of th orrect explanato ugh each resisto ch resistor rema	ne assertion. bin of the assertion. or is the same when connected is ains the same when connected is
Q.3	<ul> <li>(b), (c) and (d) as a Both A and I b) Both A and I c) A is true but d) A is false but</li> <li>Assertion (A) : series.</li> <li>Reason (R) : T parallel.</li> <li>Assertion (A) : heater.</li> </ul>	given below R are true and R are true but R is false. t R is true. The current he voltage d Alloys are co sistivity of an	d R is correct of t R is not the c t flowing thro rop across ea ommonly used	explanation of th orrect explanato ugh each resisto ch resistor rema l in electrical hea ally higher than t	ne assertion.
Q.3	<ul> <li>(b), (c) and (d) as a Both A and I b) Both A and I c) A is true but d) A is false bu</li> <li>Assertion (A) : series.</li> <li>Reason (R) : T parallel.</li> <li>Assertion (A) : heater.</li> <li>Reason (R): Reason (R): Reason (R) and the ater.</li> </ul>	given below R are true and R are true but R is false. t R is true. The current he voltage d Alloys are co sistivity of an nelting point	d R is correct of t R is not the c t flowing thro rop across ea ommonly used alloy is genera s then their cor	explanation of th orrect explanato ugh each resisto ch resistor rema l in electrical hea ally higher than t	ne assertion. Sin of the assertion. For is the same when connected is ating the same when connected is ating devices like electric iron and that of its constituent metals but the
Q.3 Q.4:	<ul> <li>(b), (c) and (d) as a Both A and I b) Both A and I c) A is true but d) A is false but</li> <li>Assertion (A) : series.</li> <li>Reason (R) : T parallel.</li> <li>Assertion (A) : heater.</li> <li>Reason (R): Reason (R): Reason</li></ul>	given below R are true and R are true but R is false. t R is true. The current he voltage d Alloys are co sistivity of an nelting point The metals a	d R is correct of t R is not the c t flowing thro rop across ea ommonly used alloy is genera s then their cor	explanation of the orrect explanator ugh each resistor ch resistor remand l in electrical heat ally higher than the astituent metals.	ne assertion. Sin of the assertion. For is the same when connected is ating the same when connected is ating devices like electric iron and that of its constituent metals but the







